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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/000,440	10/30/2001	Gerald H. Johnson	1495-US	9174

7590 02/23/2004

Legal Department
Teradyne, Inc.
321 Harrison Avenue
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EXAMINER	
TRA, ANH QUAN	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/000,440	JOHNSON, GERALD H.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 09/15/2003. Applicant's arguments have been fully considered, but they are not persuasive.

Specification

1. The amendment filed 09/15/2003 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "a first control path having a predetermined level of linear compensation"; "first control loop 20 having a pre-set level of linear compensation"...etc.

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-7 and 9-16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The original specification fails to teach "a first control path having a predetermined level of linear compensation".

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 8, 9 and 17-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 is indefinite because it is unclear how the means recited in line 4 can statically compensating the error signal since it receiving a feedback signal from the output. The output of the means will be varied in responsive to the varied output signal.

Similar rejection for claims 17-19.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 4, 5, 10, 13, 14, 17 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Takenaka (USP 5504452).

As to claim 1, Takenada discloses in figure 2 control loop circuit for optimizing a power supply output under varying load conditions (the limitation "under varying load conditions" is seen as intended use limitation, and Takenaka figure 2 is capable of providing supply voltage under varying load condition), the power supply having a main loop amplifier (12) and an output stage (24, 26) (column 4, lines 48, defines VNN as "an output voltage") to generate the output, the control loop circuit including: a first control path (12, 23, 24, 26) having predetermined level of linear compensation (since the voltage level of the COMP signal is either high constantly of

low constantly, the current going through transistor 21 is constant (linear) when transistor 21 is on. Thus, transistor 21 having predetermined linear compensation), the first control path coupled to the output (VNN) and having an error amplifier (23), the error amplifier operative to generate an error signal (COMP) for presentation to the main loop amplifier, the error signal representing the difference between a desired output (Vref) and a sensed output; and a second control path (15, 16) coupled to the error amplifier output and responsive to the error signal to generate a second compensation signal, the dynamic control path having an output coupled to the main loop amplifier output.

As to claim 4, figure 2 the second control path is disposed in parallel with the first control path.

As to claim 5, figure 2 shows the second control path is selectively activated when the error signal is greater than a predetermined threshold (transistor 32 is active when the COMP signal is greater than the threshold of the p-channel transistor in inverter 33).

As to claim 10, figure 2 shows a power supply system including: a main loop amplifier (12) circuit; an output stage (24, 26) (column 4, lines 48) disposed in cascade with the main loop amplifier circuit; and a control loop circuit, the control loop circuit including a first control path (12, 23, 24, 26) having a predetermined level of linear compensation, the first control path coupled to the output stage (24, 26) and having an error amplifier (23), the error amplifier operative to generate an error signal for presentation to the main loop amplifier, the error signal representing the difference between a desired output (Vref) and a sensed output; and a second control path (16) coupled to the error amplifier output and responsive to the error signal to

generate a dynamic compensation signal, the second control path having an output coupled to the main loop amplifier output.

As to claim 13, figure 2 shows the second control path is disposed in parallel with the first control path.

As to claim 14, figure 2 shows the second control path is selectively activated when the error signal is greater than a predetermined threshold (transistor 32 is active when the COMP signal is greater than the threshold of the p-channel transistor in inverter 33).

As to claim 17, figure 2 shows a method of controlling the output of a DUT power supply (the limitation DUT is seen as intended use, circuit figure 2 is capable of providing power supply to DUT), the method including the steps of: generating a statically compensated error signal (output of 12) (current going through 12 is constant when transistor 12 is on) based on the difference between the desired power supply (Vref) output and the actual power supply output (VNN); producing a dynamically compensated error signal (output of 15) in parallel with the static error signal; and summing the static error signal and dynamic error signal to create an optimal compensation signal.

As to claim 18, figure 2 shows the producing step is dependent on the magnitude of the statically compensated error signal being above a pre-set threshold (the threshold of the p-channel transistor in 33).

Allowable Subject Matter

8. Claims 2, 3, 6, 7, 11, 12, 15, 16 and 19 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, first and second paragraphs, set forth in this Office action and

to include all of the limitations of the base claim and any intervening claims and if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 8 and 9 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, first and second paragraph, set forth in this Office action.

Claims 2, 3, 6, 7, 11, 15, 16 and 19 would be allowable because the prior art fails to teach or suggest a circuit, and method thereof, (such as figure 2) having a dynamic control path (72), the dynamic control path includes: input conversion circuitry (ADC1) for converting the error signal (output of 32) into a digital signal, a digital-signal-processor (DSP) coupled to the conversion circuitry; a look-up table (memory) for storing optimal compensation signal responses to detected error signals, the DSP operative in response to the digitized error signal to access the look-up table and identify the optimal compensation signal, and generating the optimal signal; and output conversion circuitry (DAC2, DAC3) for feeding the optimal signal to the main loop amplifier output.

Claims 8 and 9 would be allowable because the limitation "means for statically generating an error signal' is the means plus function limitation. Clearly, Takenaka's error amplifier circuit (23) does not have similar structure, nor have equivalent function with Applicant's error amplifier circuit (35 U.S.C. 112, sixth paragraph and MPEP § 2181 through § 2186).

Response to Arguments

Applicant states that "Takenaka does not discloses nor suggest any form of changing compensation for his circuit". The Examiner respectfully disagrees. Transistor 12 is for ensuring the voltage at node VNN equal to Vref. Thus, transistor 12 is for compensating the voltage

changes at node VNN. Applicant further states that "the reference teach the use of single control loop while claim 1 recites first and second control loops". Takenaka's figure 2 shows a circuit having two loops. Loop comprising 12, 22 and 23 and loop comprising 15, 16, 22 and 23.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Terry D. Cunningham
Primary Examiner

February 23, 2004